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S75PL-N MirrorBit™ ORNAND™ MCPs

Stacked Multi-Chip Product (MCP)
S29PL-N: CMOS 3.0 Volt-only Simultaneous Read/Write, Page-mode Flash Memory (NOR Interface)
S30ML-P: ORNAND Flash (NAND Interface)
3V pSRAM

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S75PL-N_00 **Revision** 01E **Issue Date** April 21, 2006

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Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

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Data Sheet *(Advance Information)*

Features

- **Speed**
  - PL-N: 70 ns (initial access, 30 ns page access)
  - ML-P: 30 ns (page access)
  - pSRAM: 70 ns
- **107-Ball Fine-Pitch Ball Grid Array (FBGA)**
  - 9 x 12 x 1.4mm for ML512P based MCP's
  - 11 x 13 x 1.4mm for ML01GP based MCPs
- **Operating Temperature Range**
  - Temperature Range of –25°C to +85°C

General Description

This document contains information for the S75PL-N MirrorBit MCP product. TheS75PL-N product consists of the following devices:

- S29PL-N
- S30ML-P
- 3 V pSRAM

Flash/RAM Combinations Table

S29PL127N +	pSRAM Density	
	32 Mb	64 Mb
S30ML512P	S75PL127NBF	
S30ML01GP		

Product Selector Guide

Device	pSRAM Density	pSRAM Type
S75PL127NBF	32 Mb	pSRAM Type 7

For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number (PID)
S29PL-N	S29PL-N_M0
S30ML-P	S30ML-GP_00
32M pSRAM Type 7	pSRAM_29

Publication Number S75PL-N_00 **Revision 01E** **Issue Date** April 21, 2006

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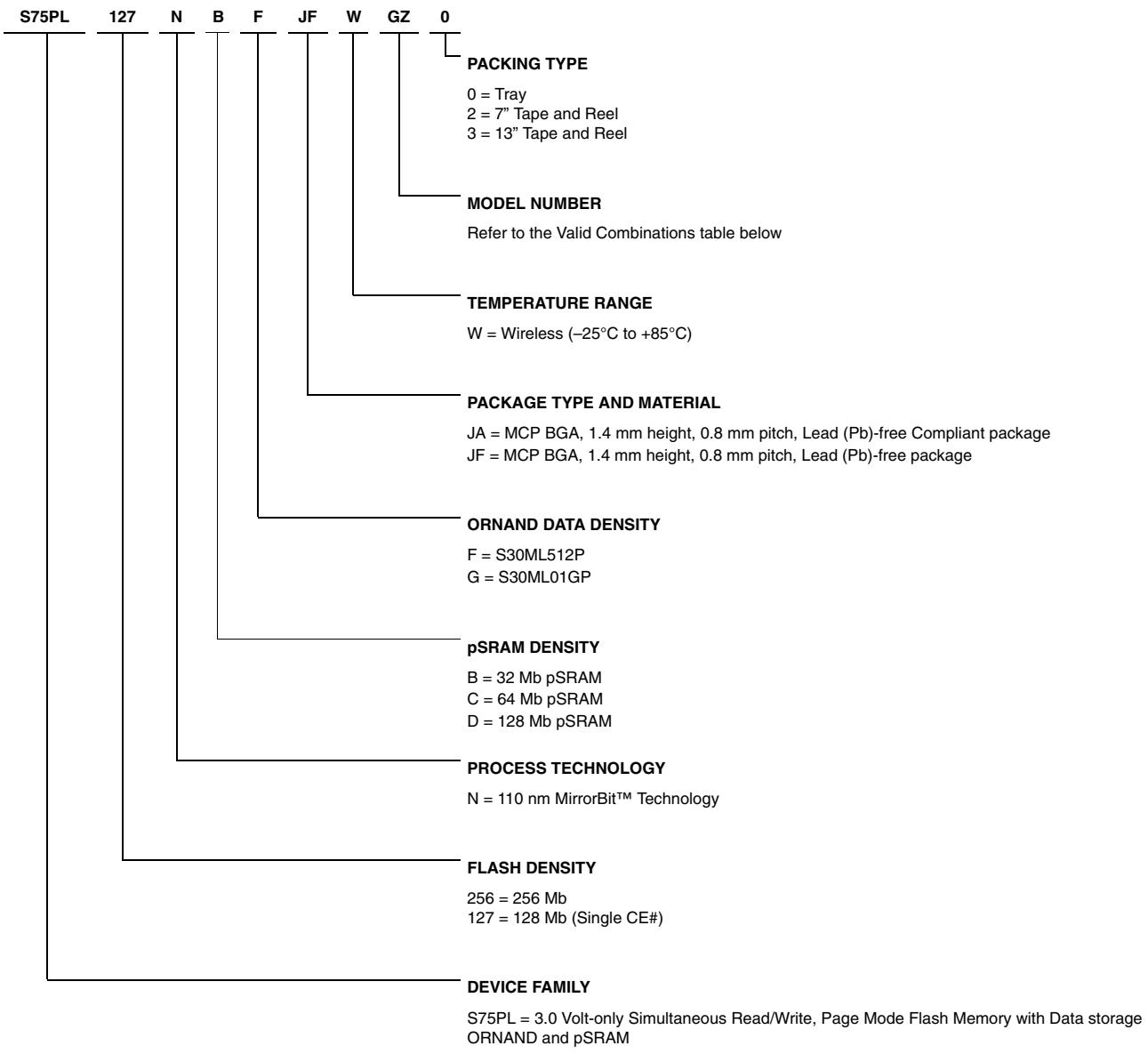
1. Ordering Information

The ordering part number is formed by a valid combination of the following:


S75PL 127 N B F JF W GZ 0
PACKING TYPE
0 = Tray
2 = 7” Tape and Reel
3 = 13” Tape and Reel
MODEL NUMBER
Refer to the Valid Combinations table below
TEMPERATURE RANGE
W = Wireless (–25°C to +85°C)
PACKAGE TYPE AND MATERIAL
JA = MCP BGA, 1.4 mm height, 0.8 mm pitch, Lead (Pb)-free Compliant package
JF = MCP BGA, 1.4 mm height, 0.8 mm pitch, Lead (Pb)-free package
ORNAND DATA DENSITY
F = S30ML512P
G = S30ML01GP
pSRAM DENSITY
B = 32 Mb pSRAM
C = 64 Mb pSRAM
D = 128 Mb pSRAM
PROCESS TECHNOLOGY
N = 110 nm MirrorBit™ Technology
FLASH DENSITY
256 = 256 Mb
127 = 128 Mb (Single CE#)
DEVICE FAMILY
S75PL = 3.0 Volt-only Simultaneous Read/Write, Page Mode Flash Memory with Data storage ORNAND and pSRAM

1.1 Valid Combinations

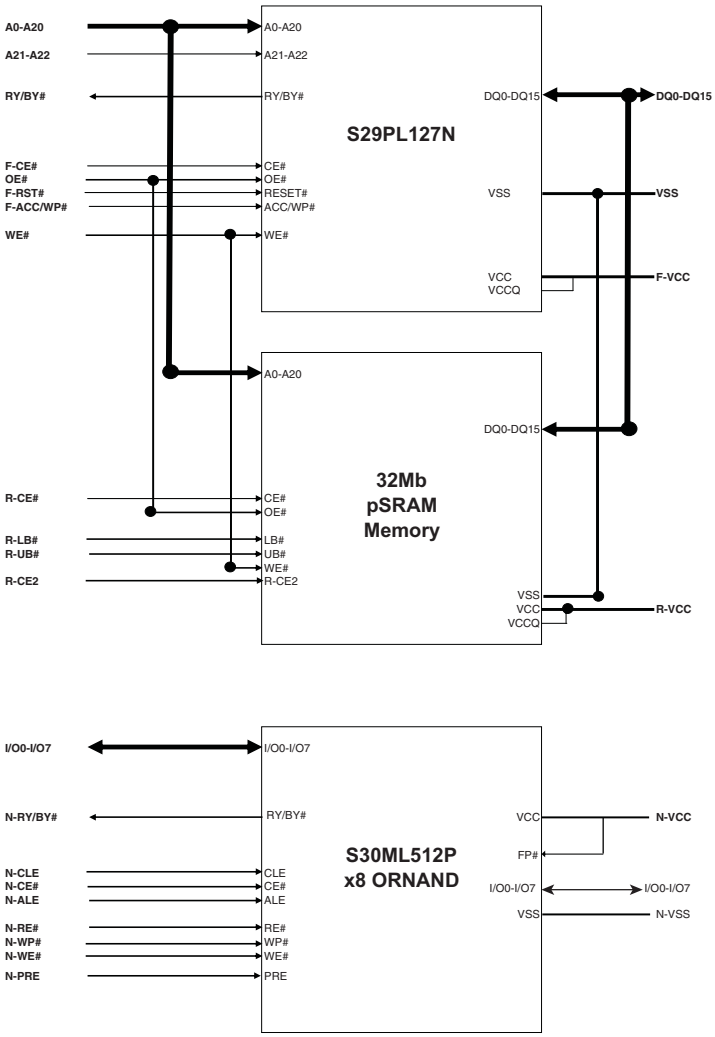
Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations								
Base Ordering Part Number (2)	**Package & Temperature**	**Model Number**	**Packing Type**	**pSRAM Type**	**PL-N Linear Mode Access Time**	**ML-P Page Mode Access Time**	**pSRAM Linear Mode Access Time**	**Package Name**
S75PL127NBF	JAW, JFW	GZ	0, 2, 3 (1), (2)	Type 7	70 ns	30 ns	70 ns	FMH107 9x12x1.4mm, 107 ball

Notes:

1. *Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading "S" and packing type designator from ordering part number.*
3. *Contact factory for availability for any of the OPNs listed since RAM type availability may vary over time.*

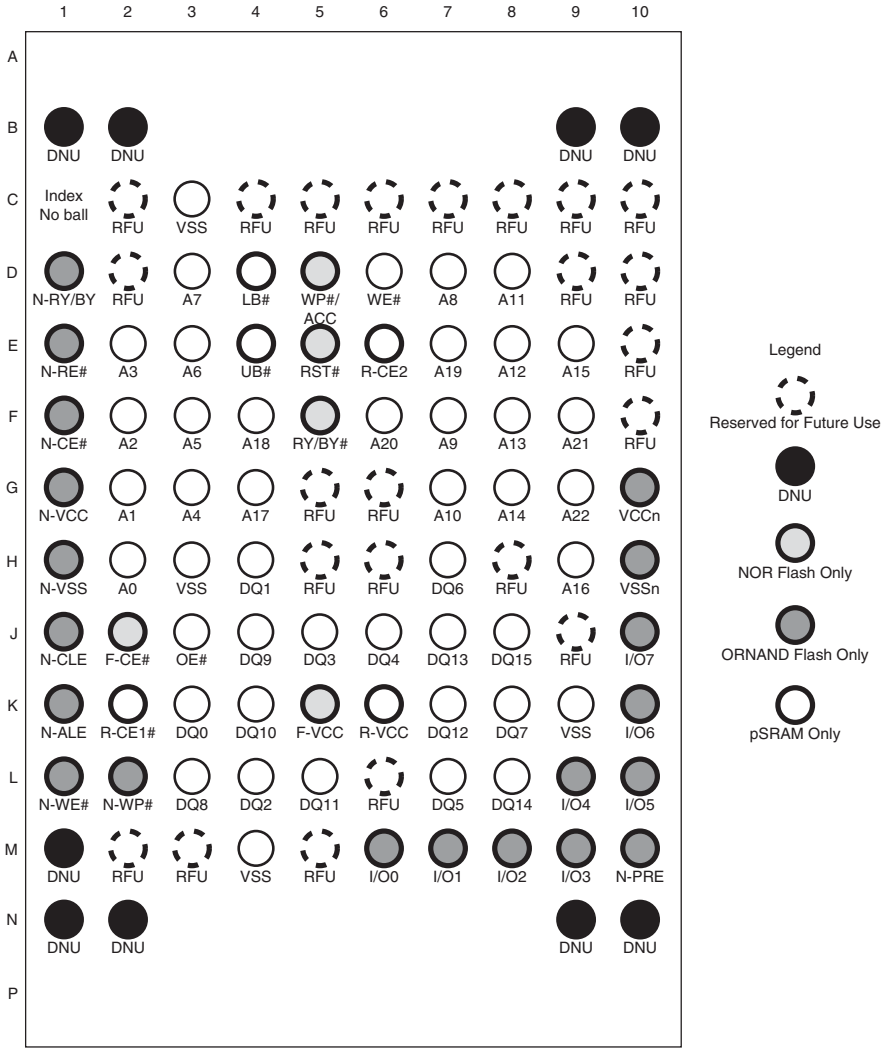
2. Block Diagram (S29PL-N and pSRAM on Bus 1, S30ML-P on Bus 2)



3. Connection Diagrams

3.1 S75PL-N Pinout

Figure 3.1 107-ball Fine-Pitch Ball Grid Array (S75PL127NBF)


1 2 3 4 5 6 7 8 9 10
A
B DNU DNU DNU DNU
C Index No ball RFU VSS RFU RFU RFU RFU RFU RFU RFU
D N-RY/BY RFU A7 LB# WP#/ ACC WE# A8 A11 RFU RFU
E N-RE# A3 A6 UB# RST# R-CE2 A19 A12 A15 RFU
F N-CE# A2 A5 A18 RY/BY# A20 A9 A13 A21 RFU
G N-VCC A1 A4 A17 RFU RFU A10 A14 A22 VCCn
H N-VSS A0 VSS DQ1 RFU RFU DQ6 RFU A16 VSSn
J N-CLE F-CE# OE# DQ9 DQ3 DQ4 DQ13 DQ15 RFU I/O7
K N-ALE R-CE1# DQ0 DQ10 F-VCC R-VCC DQ12 DQ7 VSS I/O6
L N-WE# N-WP# DQ8 DQ2 DQ11 RFU DQ5 DQ14 I/O4 I/O5
M DNU RFU RFU VSS RFU I/O0 I/O1 I/O2 I/O3 N-PRE
N DNU DNU DNU DNU
P
Legend
Reserved for Future Use
DNU
NOR Flash Only
ORNAND Flash Only
pSRAM Only

Note:
Top view—balls facing down. The addresses that are shared vary by MCP combination as shown in the table below:

	PL-N Addresses	PL-N/pSRAM Addresses
S75PL127NBF	A22-A21	A20:A0

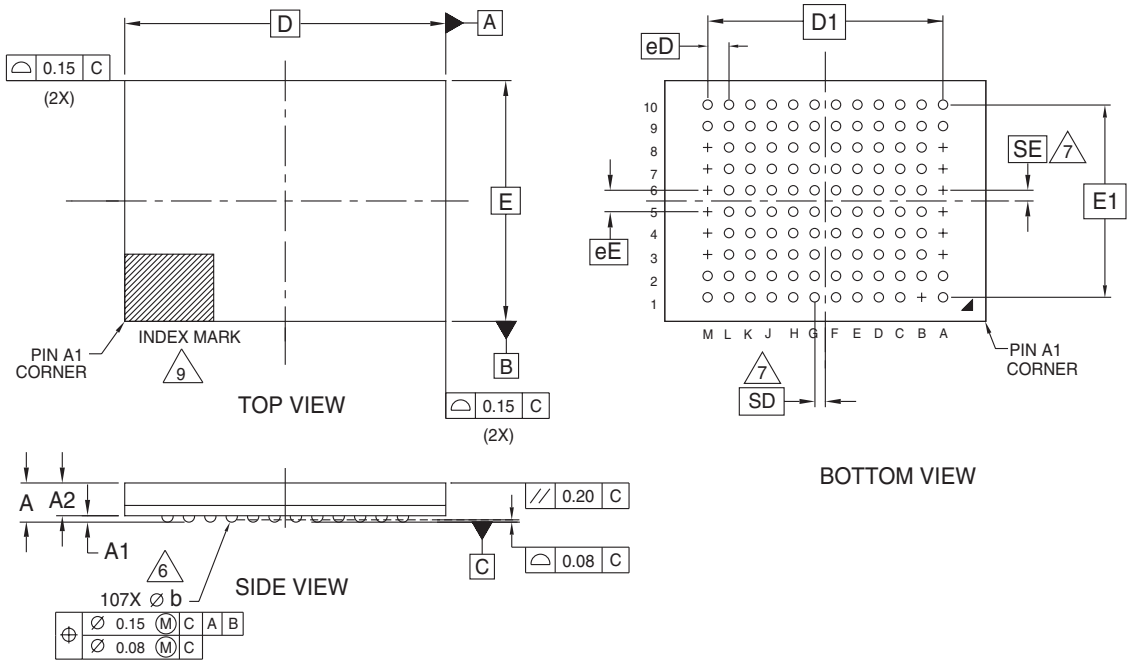
Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

3.2 FMH107—107-Ball Fine Pitch Ball Grid Array (FBGA) 9 x 12 mm package

Figure 3.2 FMH107



PACKAGE	FMH 107			
JEDEC	N/A			
D x E	12.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.94	---	1.11	BODY THICKNESS
D		12.00 BSC.		BODY SIZE
E		9.00 BSC.		BODY SIZE
D1		8.80 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		12		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		107		BALL COUNT
Ø b	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC.		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A3,A4,A5,A6,A7,A8, B1,M3,M4,M5,M6,M7,M8		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3512 \ 16-038.19 \ 8.9.05

4. Revision History

4.1 Revision A (April 21, 2006)

Initial release.

Colophon

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